What is claimed is:

1. A router apparatus wherein routing information of a first unit is mirrored to a second unit in real time, wherein at least one of the first unit and the second unit comprises at least one switching unit for transferring the routing information from the first unit to the second unit, substantially eliminating a delay associated with use of a PCI-to-PCI board for transferring the routing information.

2. The apparatus of claim 1, wherein when the routing information is stored in a first memory of a first switching unit, and wherein the first switching unit transfers the information to the second unit.

3. The apparatus of claim 2, wherein a second switching unit receives the routing information from the first switching unit and stores the routing information in a second memory of the second unit.

4. The apparatus of claim 3, wherein the second switching unit prevents signal transmission form the second unit to the second memory.

5. The apparatus of claim 2, wherein when the first memory is loaded, the first switching unit transfers any signal transferred from the first unit to the second unit.

6. The apparatus of claim 5, wherein the second switching unit prevents data from being loaded from the second memory.

7. The apparatus of claim 1, wherein the first unit comprises a first programmable switch and the second unit comprises a second programmable switch.

8. The apparatus of claim 7, wherein the first and second switching units are structural equivalents.

9. The apparatus of claim 7, wherein the first and second switching units are functional equivalents.

10. A routing redundancy apparatus comprising:

a first unit for storing routing information in a first memory and for simultaneously transferring the routing information to a second unit by using a first switching unit; and

a second unit for receiving the routing information by way a second switching unit and storing it in a second memory.

11. The apparatus of claim 10, wherein while the routing information is stored in the second memory, the second switching unit prevents signal transmission to the second memory.

12. The apparatus of claim 10, wherein when the first memory is loaded, the first switching unit prevents signal transmission form the first unit to the second unit.

13. The apparatus of claim 12, wherein the second switching unit of second unit prevents the second memory from being loaded.

14. The apparatus of claim 10, wherein the first and second switching units are programmable switches.

15. The apparatus of claim 10, wherein the first and second switching units have substantially same structural configuration.

16. A data redundancy system comprising:

a first switching unit;

a second switching unit;

a first unit comprising a first memory for storing routing information; and

a second unit comprising a second memory for storing routing information transferred from the first unit.

17. The system of claim 16, wherein the first unit further comprises the first switching unit.

18. The system of claim 17, wherein the second unit further comprises the second switching unit.

19. The system of claim 18, wherein the routing information is transferred from the first unit to the second unit via the first and second switching

units.

20. The system of claim 19, wherein the routing information stored in the first memory is transferred via the first and second switching units to the second memory.

21. The system of claim 16 wherein the first switching unit comprises:

at least one multiplexer; and

at least one tristate output buffer in communication with the at least one multiplexer;

wherein the first switching unit is configured to connect to a plurality of external devices to route a signal inputted from a first device to a second device, according to control information.

22. The system of claim 21, wherein the at least one multiplexer is a 2:1 multiplexer comprising:

two input terminals;

one output terminal; and

one control terminal responsive to a select signal.

23. The system of claim 22, wherein when the select signal is in a first state, the at least one multiplexer outputs a first signal, and when the select signal is in a second state, the at least one multiplexer outputs a second signal.

24. The system of claim 22, wherein the at least one tristate output

buffer is connected to the output terminal of the at least one multiplexer, wherein when the select signal is equal to a first value, the tristate output buffer is in an output-enable state, and when the select signal is equal to a second value, the tristate output buffer is in an output-disable state.

25. A method of providing data redundancy in a routing system having a first switching unit, a second switching unit, a first unit comprising a first memory, and a second unit comprising a second memory, the method comprising:

loading the first memory with routing information received by the first unit;

transferring the routing information from the first board to the second unit via the first switching unit in communication with the second switching unit; and

loading the second memory with the routing information.

26. The method of claim 25, wherein the first unit further comprises the first switching unit.

27. The method of claim 26, wherein the second unit further comprises the second switching unit.

28. The method of claim 25, wherein the first switching unit comprises:

at least one multiplexer; and

at least one tristate output buffer in communication with the at least one multiplexer;

wherein the first switching unit is configured to connect to a plurality of

external devices to route a signal inputted from a first device to a second device, based on control signals.

29. The method of claim 25, wherein the at least one multiplexer is a 2:1 multiplexer comprising:

two input terminals;

one output terminal; and

one control terminal responsive to a select signal.

30. The method of claim 29, wherein when a select signal is in a first state, the at least one multiplexer outputs a first signal, and when the select signal is in a second state, the at least one multiplexer outputs a second signal.